CE-6785-86

B. E. III (Sem. V) (EC/ECC) Examination

November / December – 2008

Pulse & Switching Circuits

Time : 3 Hours] [Total Marks : 100

CE–6785

Instructions :

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :
☛ B. E. 3 (Sem. 5) (EC/ECC)

Name of the Subject :
☛ Pulse & Switching Circuits

☛ Subject Code No. : 6 7 8 5 ☛ Section No. (1, 2,.....) : 1

Seat No. :

Student's Signature

(2) Attempt **all** questions.

(3) Assume data if **necessary.**

(4) Answers to the **two** section must be written in **separate** answer books.

(5) Figures to the **right** indicate full marks.

1 (a) Answer the following : 10

(1) Resistance R = 1 M Ω; capacitance C = 15 PF. In RC circuit what will be the rise time of output waveform for squarewave input consider Lowpass RC circuit. 2

(2) Draw the waveform representation for V_D if $V_i = V_m \sin wt$. V_D is the voltage across diode. 2

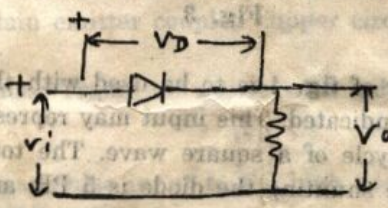

Fig. 1

(3) Draw the steady state output across diode if $V_i = V_m \sin wt$. 2

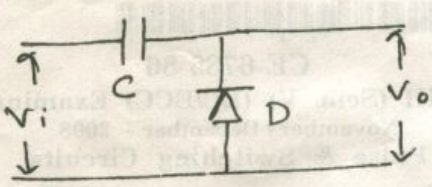

Fig. 2

(4) What is the disadvantage of having a diode as a series element in a clipper circuit ? **2**

(5) Define Ramp signal. **1**

(6) How much change in voltage (break down voltage) of diode if temp. rise 1°C.

(b) Explain attenuator in detail. Compute and draw to scale the output waveform for : **10**

(1) C = 50 PF

(2) C = 75 PF

(3) C = 25 PF.

The input is a 20 V step. consider **fig. 3.**

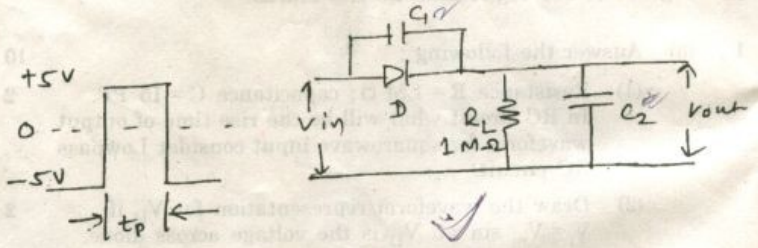

Fig. 3

2 (a) The clipper of **fig. 4** is to be used with the input waveform indicated. This input may represent a pulse of half a cycle of a square wave. The total effective capacitance shunting the diode is 5 PF; and the total capacitance shunting the output load resistance is 20 PF. Find the output waveform, assuming that the back resistance is infinite. **8**

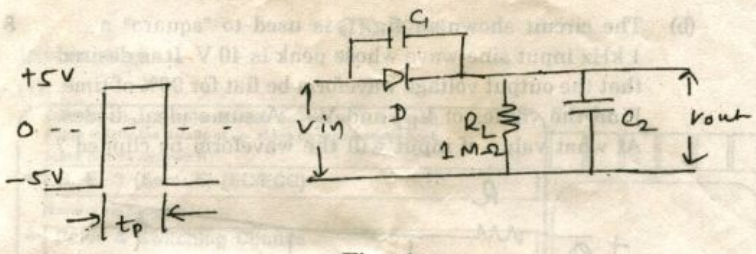

Fig. 4

(b) What is a problem with basic clamping circuit. Give the solution and explain practical clamping circuit in detail. **7**

OR

2 (a) In the restorer circuit shown in **fig. 5**. $R_f = 0.1\ k\Omega$, $R_r = \alpha$, $V_8 = 0$ and $R = 100\ k\ \Omega$. The waveform is a rectangular wave with $V = 30\ V$ $T_1 = 50\ \mu s$. and $T_2 = 1000\ \mu s$. **8**

(i) $R_s = 0$ and that C is arbitrarily large. Calculate and sketch the steady state output V_0.

(ii) Repeat (i) if $Rs = 0.1\ \Omega$.

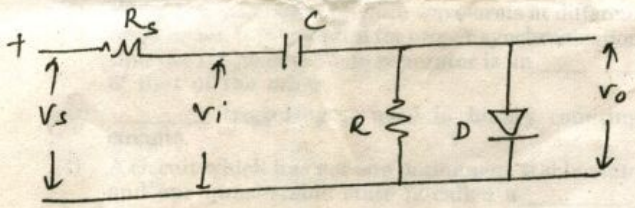

Fig. 5

(b) Explain emitter coupled clipper circuit. **7**

3 (a) Discuss "Transistor switch with inductive load. **7**

OR

(a) Discuss pulse input to RC high pass circuit with **7**

(i) RC >> tp

(ii) RC << tp

where tp is pulse duration

and RC is time constent.

(b) The circuit shown in **fig. 6** is used to "square" a 1 kHz input sine wave whose peak is 40 V. It is desired that the output voltage waveform be flat for 90% of time. Find the values of V_{R1} and V_{R2}. Assume ideal diodes. At what value of input will the waveform be clipped ? 8

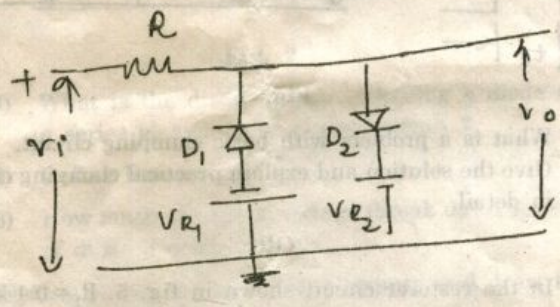

Fig. 6

CE-6786

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(2) Attempt **all** questions.

(3) Assume data if **necessary**.

(4) Answers to the **two** section must be written in **separate** answer books.

(5) Figures to the **right** indicate full marks.

(6) Use of scientific calculator Fx-82/83, Fx.100 or equivalent of other companies are allowed.

4 (a) Answer the following : 10

(1) The reciprocal of the resolving time of the flip-flop is the _____ at which the binary will respond.

(2) When two generators produce waveforms at different frequencies, it is essential for proper synchronization that the frequency of one generator is an _____ of that of the other.

(3) _____ triggering is used in binary counting circuits.

(4) A circuit which has got one permanent stable state and one quasi-stable state is called a _____.

(5) An _____ multivibrator can be used as a voltage to frequency converter.

(6) Define resolving time.

(7) Define Blocked condition.

(8) _____ is defined as the input voltage at which Q_1 starts conducting.

(9) _____ are used to maintain a constant output swing in a bistable multivibrator.

(10) Loop gain will be _____ if either of the two devices is below cutoff or if either of the two devices is in saturation.

(b) (1) Explain Non-saturating binary. 5

(2) Explain triggering symmetrically through a unilateral device. 5

5 (a) For the fixed biased binary shown, $h_{FE(min)} = 40$, $V_{CC} = 18$ V, $V_{BB} = 6$ V, V = 6 V, $R_C = 1.5$ k Ω, $R_1 = 5$ k Ω, $R_2 = 25$ k Ω. Neglect the drop across the forward biased junctions. (a) verify that one transistor is in cutoff and other is in saturation. (b) What is the maximum load the bistable multivibrator can drive ? (c) If $I_{CBO} = 5$ μA at 20°C and doubles for every 10°C rise in the temperature, find the maximum temperature at which one device will still remain in cutoff and other in saturation. 9

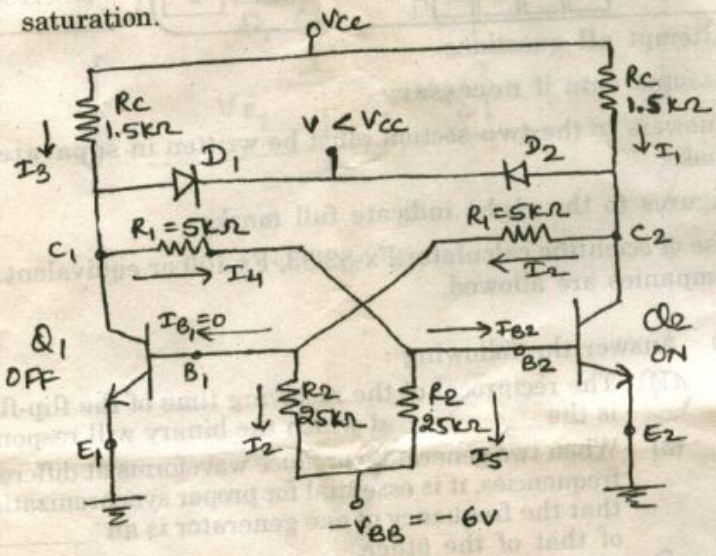

Fig. 7

(b) Explain commutating capacitors. Also state the methods of improving the resolution. 6

OR

5 (a) A self biased bistable multivibrator using a n-p-n transistor having $V_{CE(sat)} = 0.4$ V $V_{BE(sat)} = 0.8$ V, $R_C = 4.7$ k Ω, $R_1 = 30$ kΩ, $R_2 = 15$ kΩ, $R_E = 0.39$ kΩ, $h_{FE} = 25$, $V_{CC} = 20$V. It has zero base to emitter voltage for cut off. Find out : 10

(i) Stable state voltages and currents.

(ii) Maximum load that the binary can drive and still have one transistor in saturation while other is below cutoff.

(iii) The maximum value of I_{CBO} required to reach the condition that neither device is OFF.

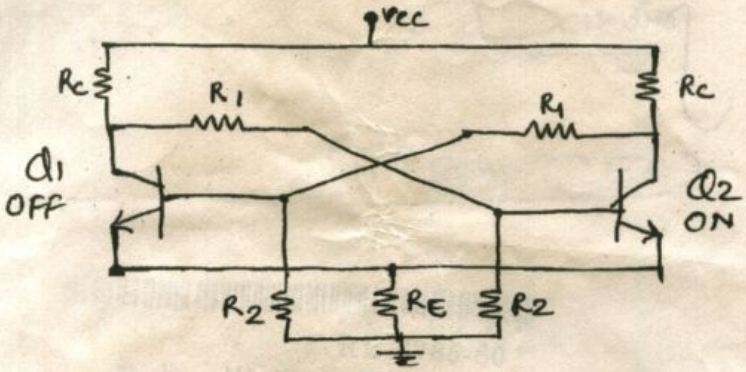

Fig. 7

(b) Write a short note on DCTL. 5

6 (a) Draw and explain waveform of collector coupled monostable multivibrator. 7

(b) Silicon n-p-n transistor with $h_{FE(min)} = 40$ are available. Design an astable multivibrator to generate a square wave of 1 kHz frequency with a duty cycle of 25%. 8

OR

6 (a) Explain Astable multivibrator as V to F converter. 8

(b) Explain gated astable multivibrator. 4

(c) For the astable multivibrator shown, $R_1 = 20\ k\Omega$, $R_2 = 10\ k\Omega$, $C_1 = 0.02\ \mu F$, $C_2 = 0.015\ \mu F$, find the frequency of oscillation and duty cycle of output waveform. 3

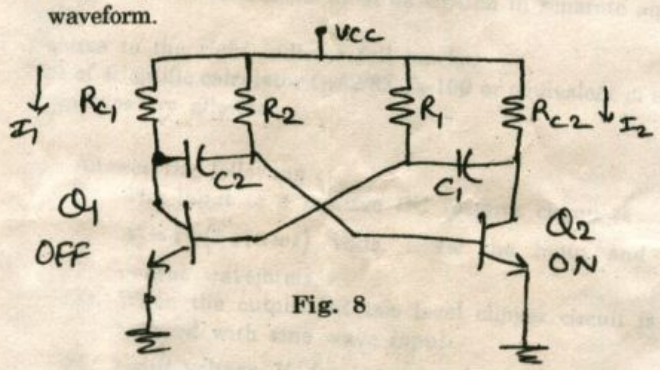

Fig. 8