R-6789-90

B. E. III (Sem. V) (EC/ECC) Examination

May / June – 2007

Digital Micro Electronics

Time : 3 Hours] [Total Marks : 100

R–6789

Instructions :

(1)

નીચે દર્શાવેલ ☛ નિશાનવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :
☛ B. E. 3 (Sem. 5) (EC/ECC)

Name of the Subject :
☛ Digital Micro Electronics

☛ Subject Code No. : 6 7 8 9 ☛ Section No. (1, 2,.....) : 1

Seat No. :

Student's Signature

(2) Attempt all questions.

(3) Figures on right indicate full marks.

(4) Assume suitable data if required.

1 (a) Attempt the following : 10

(1) Define fanout

(2) Define propagation delay

(3) State the disadvantage of DCTL logic family

(4) Fanout of the ECL gate is highest. (state true/false)

(5) What is the function of diode connected between inputs and ground in TTL ?

(6) State the advantage of HTL over DTL.

(7) What is active pull up ?

(8) Among TTL and ECL, which family has higher power dissipation ?

(9) State true/false : DTL is faster than TTL

(10) IIL is different from RTL and DTL (State true/false)

(b) (i) Explain current hogging phenomenon in DCTL. 5

(ii) Explain the methods to remove the propogation delay hazards with diagram. 5

2 (a) Draw and explain RTL NOR gate. Discuss the manufacturer's specification of RTL gates in detail. 7

(b) Draw and explain HTL NAND gate with its transfer characteristics. Also explain that the temperature sensitivity of HTL is better than DTL. 8

OR

2 (a) Draw and explain two input IC DTL NAND gate. 7

(b) Explain the basic configuration of I^2L family. 8

3 Attempt any **two** : 15

(1) Draw and explain standard two input TTL NAND gate.

(2) Calculate the static fanout for the circuit shown in Fig. 1. Assume that the NOR output voltage can drop from its nominal (high) value of –0.7V by $\Delta V = 50$ mV. Use $\beta = 100$.

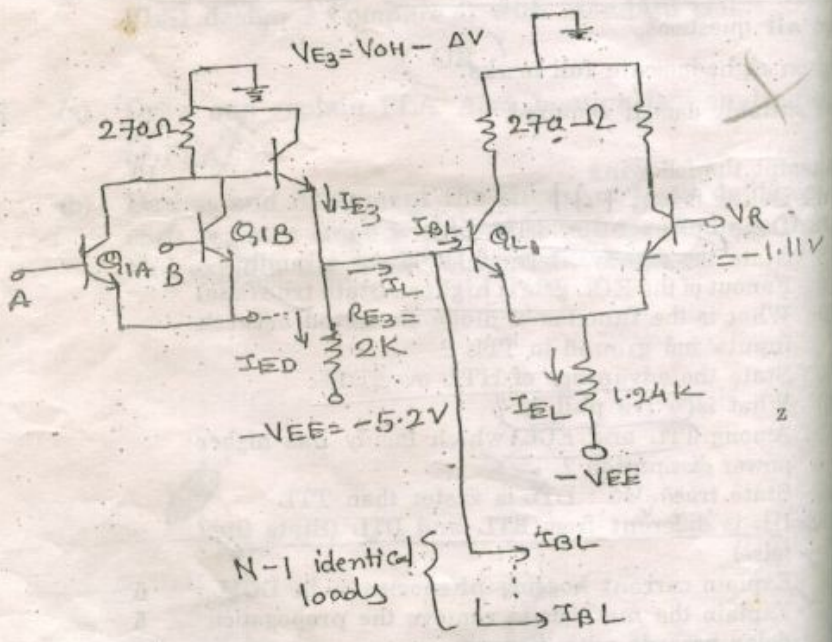

Fig. 1

(3) Explain the basic principle of ECL gate and draw an ECL NOR gate.

R–6790

Instructions :

(1)

નીચે દર્શાવેલ ← નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ← signs on your answer book.

Name of the Examination :
← B. E. 3 (Sem. 5) (EC/ECC)

Name of the Subject :
← Digital Micro Electronics

← Subject Code No. : 6 7 9 0 ← Section No. (1, 2,.....) 2

Seat No. :

Student's Signature

(2) Attempt all questions.

(3) Figures on right indicate full marks.

(4) Assume suitable data if required.

4 (a) Attempt any five : (each of 2 marks) 10

(1) Mention interfacing criteria to interface TTL CMOS ckt.

(2) What is the importance of W/L ratio in CMOS inverter ?

(3) What is BiCMOS Totem-pole gate ? What does transition do at output stage of circuit ?

(4) Why MOS logic is mainly used for LSI and VLSI applications ?

(5) Some information is stored in an EPROM, which is required to be modified, how will you do it ?

(6) Differentiate between random access memory and sequentially accessed memory from the point of view of speed of operation.

(7) What are the main advantages of using PLAs for realizing combinational logic function over logic gates ?

(b) Compare TTL, BiCMOS and CMOS logic family with respect to propagation delay and power dissipation. Describe the importance of the bleeder resistors in BiCMOS inverter circuit with proper circuit diagram. 6

(c) Calculate the rise time of N channel MOSFET. If load capacitance is 5 PF
Transconductance parameter is 20 $\mu A/V^2$
Supply voltage is 12 V
Threshold voltage is 0.7 V 4

5 (a) Design and implement the following Boolean expression using PMOS and also list out No. of transistors required for implementations 8

(1) $V_D = \bar{A} \cdot (\bar{B} + \bar{C})$

(2) $V_D = \bar{A} + \bar{B}\,\bar{C}$

(b) What is memory refreshing ? Which type of transistor RAM cell use refresh circuit ? Draw and explain such a cell with its proper working. 5

OR

5 (a) Explain rise time and fall time in CMOS gate. 8

(b) It is desired to combine separate 2 k × 8 PROM to produce a total capacity of 8 k × 8. How many PROM chips are needed ? How many address bus lines are required ? 5

(c) Draw NMOS NAND gate. 2

6 (a) Which parameter in fabrication play an important role to make an erasable PROM ? Explain the construction and working of EPROM. 7

(b) Draw the structure of the circuit which requires programmable AND gates and programmable OR gates. Explain its operations in brief. 8

OR

6 (a) Explain programmable logic device need. What is the significance of CMOS logic family in VLSI design ? Explain CMOS gate array approach with an appropriate diagram. 8

(b) Draw and explain DRAM one bit transistor memory cell. 7