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5489/5490

B. E. III (Sem. VI) (EC & ECC) Examination

October / November – 2005

Computer Architecture & Organization

Time : **3** Hours] [Total Marks : **100**

Instructions :

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ **B.E. - III (Sem. VI) (EC & ECC)**

Name of the Subject :

☛ **Computer Architecture & Organization**

☛Subject Code No. : **5 4 8 9** ☛Section No. (1, 2,.....) : **Nil**

Seat No. :

Student's Signature

1 Answer following questions : (any **six**) **18**

(a) What is Interrupt ? Explain types of Interrupt.

(b) What is the difference between direct and indirect address instruction ? How many memory references are needed for each type of instruction to bring an operand into a processor register ?

(c) Covert following infix notation to reverse polish notation

(i) (A + B * (C * D + E – F))/(G + H * K)

(ii) A + (B * C + (D * E / F / G) * H) * I

(d) Show register transfer statement for following instructions :

(i) ADM (Add with Memory)

(ii) CIL (Circular left)

(e) What must be the address field of an indexed addressing mode instruction to make it the same as a register indirect mode instruction.

(f) Explain Memory Interleaving.

(g) Give an example that uses delayed branch with 3-segment pipeline.

(h) Why should the sign of the remainder after a division be the same as the sign of the dividend ?

2 (a) Explain Interrupt Cycle with flowchart. 8

(b) Specify the instruction format of a computer that can perform following operation : 4

$D \leftarrow$ Mem [add] + S

(c) An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if addressing mode of the instruction is (a) direct (b) immediate; (c) relative (d) register indirect (e) index with R1 as the index register. (Specify your answer). 4

3 (a) Enlist three major Pipeline conflicts. Explain each of them. 6

(b) Explain selection of address for control memory. 6

(c) Explain the difference between hardwired control and micro programmed control memory. Is it possible to have a hardwired control associated with a control memory ? 4

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Name of the Examination :

☛ B.E. - III (Sem. VI) (Computer)

Name of the Subject :

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4 (a) Derive an algorithm in flowchart form for the non-restoring method of fixed point binary division. **8**

OR

(a) Explain multiplication algorithm with flowchart for binary floating point numbers. **8**

(b) A virtual memory has page size of 512 words. There are 16 pages and 4 blocks. The associative memory page table contains following entries : **8**

Page	Block
2	3
8	1
13	2
5	0

Make a list of all virtual addresses that will cause page fault.

(c) What is polling ? How is it used in interrupt serving ? **2**

5 (a) The access time of cache memory is 200 ns and that of main memory is 2000ns. It is estimated that 70% of the memory requests are for read and remaining 30% for write. The hit ratio for read accesses only is 0.9. A write through procedure is used. **10**

(i) What is the average access time of the system considering only memory read cycle ?

(ii) What is the average access time of the system for both read and write requests ?

What is the hit ratio taking into consideration the write cycles ?

(b) What programming steps are required to check when source interrupts the computer while it is still being serviced by previous interrupt request from the same source ? 4

(c) Design parallel priority interrupts h/w for a system with eight interrupt. 8

6 Write short notes on : (any **four**) **16**

(a) FIFO-Buffer

(b) CPU-IOP communication

(c) Array Multiplier

(d) Cache Coherence

(e) Set Associative Mapping.
