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DE-5419-5420

B. E. - III (EC & ECC) (Sem. VI) Examination

November / December – 2006

Computer Architecture & Organization

Time : 3 Hours] **[Total Marks : 100**

DE-5419

Instructions :

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ B. E. - 3 (EC & ECC) (SEM. 6)

Name of the Subject :

☛ COMPUTER ARCHITECTURE & ORGANIZATION

☛ Subject Code No. : 5 4 1 9 ☛ Section No. (1, 2,.....) : 1

Seat No. :

Student's Signature

(2) Answer the two sections in separate answer books.

(3) Figures to the **right** indicate necessary marks.

(4) Make necessary assumptions and clearly mention them.

1 Answer the following questions : (any **six**) **18**

(1) Define terms : 3

(i) Instruction Code

(ii) Operation Code

(iii) Micro Instruction.

(2) Why in DMA Controller Read and Write lines are bidirectional ?

(3) Discuss basic instruction formats. 3

(4) Write Micro operations for the following set of instructions :

(i) PUSH 2

(ii) ADD

(iii) ISZ.

SP ← SP + 1
M [SP] ← DR
If (SP = 0) then (FULL ← 1)
EMPTY ← 0

(5) What is the difference between Isolated I/O and Memory mapped I/O ?

(6) Convert the following arithmetic expressions from reverse polish notation to infix notation :

(a) A B C * / D – E F / +

(b) A B C D E * / – +

(7) What is the non-restoring method for binary division ?

2 (a) Design an array multiplier that multiply two 4-bit numbers. Use AND gates and binary address. 4

(b) Explain stack organization with related micro instruction and give example. 12

OR

(b) A two word instruction is stored in memory at an address designated by the symbol W. The address field of the instruction (stored at W + 1) is designated by the symbol Y, the operand used during the execution of the instruction is stored at an address symbolized by Z. An index register contains the value X. State how Z is calculated from the other address if the addressing mode of the instruction is : 12

(i) Direct

(ii) Indirect

(iii) Relative

(iv) Indexed.

3 Attempt any **four** : 16

(1) RISC Vs CISC characteristic

(2) Interrupt Cycle using Flowchart

(3) Explain Micro Program Sequencer

(4) Memory Interleaving

(5) Derive speed of ratio of pipeline processing over an equivalent nonpipeline processing.

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Name of the Subject :

☛ COMPUTER ARCHITECTURE & ORGANIZATION

☛ Subject Code No. : 5 4 2 0 ☛ Section No. (1, 2,.....) : 2

Seat No. :

Student's Signature

(2) Answer the two sections in **separate** answer books.

(3) Figures to the **right** indicate necessary marks.

(4) Make necessary assumptions and clearly mention them.

4 (a) A digital computer has a memory unit of 64 K * 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of four words : **6**

(i) How many bits are there in the tag, index, block, and word fields of the address format ?

(ii) How many bits are there in each, and how are they divided into functions ? Include a valid bit.

(iii) How many blocks can the cache accommodate ?

(b) A virtual memory system has an address space of 8K words, a memory space of 3K words, and page and block sizes of 1K words. The following page reference changes occur during a given time interval. (Only page changes are listed. If the same page is referenced again, it is not listed twice). **6**

7, 0, 1, 2, 0, 3, 0, 4 , 2, 3 0, 3, 2, 1, 2, 0, 1,7, 0,1

Determine the three pages that are resident in main memory after each page reference change if the replacement algorithm used is (i) FIFO (b) LRU (iii) MRU (Most Recently Used).

(c) Discuss memory hierarchy in computer system. **6**
Discuss the purpose of each memory in that hierarchy.

OR

(c) Discuss different data transfer modes for peripherals. **6**

5 (a) Explain the Booth Multiplication Algorithm with flowchart and example. 8

(b) Explain addition and subtraction of floating point numbers with flowchart. 8

OR

5 (a) Explain division algorithm with flowchart for floating point binary numbers. 8

(b) Explain with flowchart, Algorithm for decimal division. 8

6 Attempt any **four** : 16

(1) Input-Output Processor (IOP)

(2) Parallel priority interrupt

(3) Mutual exclusion with semaphore

(4) Page Replacement Techniques

(5) Loosely Coupled and Tightly coupled

(6) Associative Memory.
