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DM-7083-84

B. E. III (EC) (Sem. VI) Examination

January - 2008

Computer Architecture & Organization

Time : 3 Hours]

[Total Marks : 100

DM-7083

Instructions :

(1)

नीचे दशांशव - निशुद्धिवाणी विगतो उतरवादी पर सवश्य लम्दी.  
Fillup strictly the details of signs on your answer book.

Name of the Examination :

Name of the Subject :

Subject Code No. :     Section No. (1, 2,.....) :

Seat No. :

Student's Signature

- (2) Use separate answer sheet for separate section.
- (3) Make assumption whenever required.
- (4) Numbers on the right indicate marks.

1 Answer Following Questions. (Any Six)

18

1 Explain the following instruction with register transfer statements.

- a) BSA (Branch & Save Address)
- b) Interrupt

AR ← 0, TR ← PC  
M[AR] ← TR PC ← 0  
PC ← PC + 1, IEN ← 0  
R ← 0, SC ← 0

2 Convert following infix notation to reverse polish notation.

- i)  $(A - B + C * (D * E - F)) / (G + H * K)$
- ii)  $(A + B) * (C * (D + E) + F)$

3 Define Computer Architecture and Computer Organization.

4 Discuss memory hierarchy in a computer system. Explain cache memory in brief.

5 List different schemes that can be used in an instruction pipeline in order to minimize the performance degradation caused by instruction branching. Explain any two of them.

prefetch target instruction  
branch target instruction  
loop buffer  
branch prediction  
delayed branch

6 Why does DMA have high priority over the CPU when both request memory transfer?

7 Explain memory interleaving.

2 A Describe the register based CPU organization with diagram which allows manipulating any two or single register using register related instructions.

ADD :

ORG 0

NOP

READ

ADD

I

U

U

CALL INDIRECT

JMP NEXT

JMP FETCH

CD DR AD

AD

EXCHANGE: ORG 12

NOP

READ

ACTDR, DRTAC

WRITE

- B Explain Division Algorithm with flow chart for binary numbers. 8
- OR
- 2 ~~A~~ Explain Booth's Multiplication Algorithm. 8
- B Explain symbolic microinstruction and write symbolic micro program for ADD and EXCHANGE label. 3
- 3 ~~A~~ Explain micro programmed control organization. 8
- B Answer the following (Any two) 8
- (i) Explain interrupt initiated I/O.
- (ii) Formulate a six segment instruction pipeline for a computer. Specify the operation to be performed in each segment.
- ~~(iii)~~ Explain various CPU organizations.

3 types of CPU organizations

Single accumulator organization

General register organization

Stack organization

# DM-7084

**Instructions :**

(1)

<p>नीचे दृष्टवित निम्नलिखित विगत उत्तरपत्री पर अवश्य लपवत।                  Fillup strictly the details of signs on your answer book.</p> <p>Name of the Examination :  <input style="width: 90%;" type="text" value="B. E. 3 (EC) (Sem. 6)"/></p> <p>Name of the Subject :  <input style="width: 90%;" type="text" value="COMPUTER ARCHITECTURE &amp; ORGANIZATION"/></p> <p>Subject Code No. : <input style="width: 20px;" type="text" value="7"/> <input style="width: 20px;" type="text" value="0"/> <input style="width: 20px;" type="text" value="8"/> <input style="width: 20px;" type="text" value="4"/> Section No. (1, 2,.....): <input style="width: 20px;" type="text" value="2"/></p>	<p>Seat No. : <input style="width: 20px;" type="text"/> <input style="width: 20px;" type="text"/></p> <div style="border: 1px solid black; border-radius: 15px; height: 80px; margin-top: 10px; display: flex; align-items: center; justify-content: center;"> <p>Student's Signature</p> </div>
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- (2) Use separate answer sheet for separate section.
- (3) Make assumption whenever required.
- (4) Numbers on the right indicate marks.

- 4 Attempt the following.
- A What do you mean by priority interrupt? Discuss h/w priority interrupt system. 6
  - CH-10  B Explain Addition and Subtraction of signed 2's complement data with flow chart and hard ware implementation. 8
  - C Explain Flynn's classification. 4
  - 5  A Explain with an example 12
    - i) Zero Address Instruction
    - ii) One Address Instruction
    - iii) Two Address Instruction
    - iv) Three Address Instruction
  - B Explain Difference between RISC vs. CISC. 4
- OR**
- CH-10  5 A Explain division of two fixed point binary numbers in signed magnitude format. Also draw the flow chart. 10
  - B Explain HandShaking for asynchronous data transfer. 6
- 6 Attempt any four: 16
- 1 Explain Daisy chaining priority.
  - 2 Derive ratio for speedup of a pipeline processing over an equivalent non-pipeline processing.
  - 3 Explain SIMD array processors.
  - 4 Explain Microinstruction format.
- 5 Indicate weather the following constitute a control, status or data transfer command
- 1. Skip next instruction if flag is set.
  - 2. Seek a given record on the magnetic disk.
  - 3. Check if I/O device is ready.

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