AC ← AC ∧ M[AR]
AC ← AC + M[AR]
AC ← M[AR]

* B B - 5 4 1 9 - 5 5 0 0 *

# BB–5419–5420

## B. E. III (Sem. VI) (EC & ECC) Examination

**May / June – 2006**

## Computer Architecture & Organization

Time : 3 Hours] [Total Marks : **100**

## BB–5419

**Instructions :**

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
**Fillup strictly the details of ☛ signs on your answer book.**

Name of the Examination :
☛ B. E. III (Sem. VI) (EC & ECC)

Name of the Subject :
☛ Computer Architecture & Organization

☛ Subject Code No. : 5 4 1 9 ☛ Section No. (1, 2,.....) : 1

Seat No. : 1 0 5 0 5 0

Student's Signature

(3) Answser the two sections in separate answer books.
(4) Figure to the right indicate necessary marks.
(5) Make necessary assumptions and clearly mention them.

1 **Answer the following questions : (any six)** 18

(1) Discuss mapping between instruction code to microinstruction address.
(2) Write Mircooperation for the following set of instruction.
(a) LDA (b) ADD AC ← AC + DR (c) AND AC ← AC ∧ DR
AC ← M[AR]
(3) What is interrupt ? List and explain types of interrupts.
(4) Explain the difference between hardwired control and microprogrammed control.
(5) Discuss Computer architecture vs. Computer organization.
(6) Explain direct and indirect addressing mode with the help of example.
(7) Explain Von-neuman architecture.

2 (A) How many characters per second can be transmitted over a 1200- baud line in each of the following modes? (Assume character code of eight bits.) 4

a) Synchronous serial transmission.
b) Asynchronous serial transmission with two stop bits.
c) Asynchronous serial transmission with one stop bit.

(B) Explain stack organization with related micro instruction and give example. 12

OR

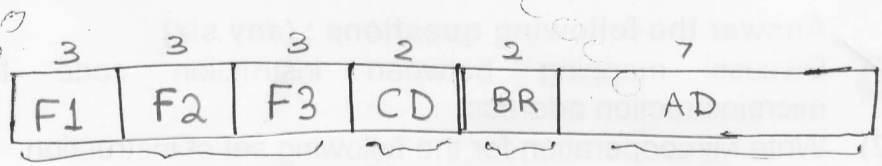
(B) Three Computers use register windows with the following characteristics. Determine the window size and total number of registers in each computer. 12

| | Computer1 | Computer2 | Computer3 |
|---|---|---|---|
| Global Registers | 10 | 8 | 16 |
| Local Registers | 10 | 8 | 16 |
| Common Registers | 6 | 8 | 16 |
| Number of windows | 8 | 4 | 16 |

3 **Write short notes:(Any Four)** 16

(1) Microinstruction Formats.
(2) Cache coherence.
(3) Hardware interlocks and Operand forwarding.
(4) RISC Vs CISC Characteristics.
(5) Memory Interleaving.

Microinstruction format




→ 20 bits in length

Divided into 4 functional parts

3 fields
$F_1$ $F_2$ $F_3$
3 micro operation fields

CD
Condition for branching

BR
Branch field

AD
Address field

# BB–5420

**Instructions :**

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
**Fillup strictly the details of ☛ signs on your answer book.**

Name of the Examination :
☛ B. E. III (Sem. VI) (EC & ECC)

Name of the Subject :
☛ Computer Architecture & Organization

☛ Subject Code No. : 5 4 2 [illegible] ☛ Section No. (1, 2,.....) : 2

Seat No. :

Student's Signature

(3) Answser the two sections in separate answer books.
(4) Figure to the right indicate necessary marks.
(5) Make necessary assumptions and clearly mention them.

**4 (A) Define the following terms :** **10**

1) Page fault
2) CAM Content addressable memory / associative memory
3) Polling
4) Bootstrap loader
5) Vectored interrupt

**(B)** A four way set-associative cache memory has four words in each set. A replacement procedure based on the least recently used (LRU) algorithm is implemented by means of 2-bit counters associated with each word in the set. A value in the range 0 to 3 is thus recorded for each word. When a hit occurs, the counter associated with the referenced word is set to 0, those counters with values originally lower than the referenced one are incremented by 1, and all others remain unchanged. If a miss occurs, the word with counter value 3 is removed, the new word is put in its place, and its counter is set to 0. The other three counters are incremented by 1. Show that this procedure works for the following sequence of word reference : A, B, C, D, B, E, D, A, C, E, C, E. (Start with A, B, C, D as the initial four words, with word A being the least recently used.) **6**

**5 (A)** Explain with flow chart 2's complement division algorithm. **8**

**(B)** Explain with flow chart, algorithm for multiplication of floating point numbers. **8**

**OR**

CH-10 ~~(A)~~ Explain with flow chart 2's complement multiplication algorithm. 8

CH-10 ~~(B)~~ Explain with flow chart, algorithm for floating point division. 8

6 **Answer the following : (Any three)** 18

M IMP
- ~~(1)~~ Associative memory
- (2) SIMD array processor
- ~~(3)~~ Daisy chaining priority — serial priority interrupt
- ~~(4)~~ CPU-IOP communication

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1) computer organization & Computer Architecture
diff bet'n micro program & micro instruction
" code
" operation
" programme

3) Diff bet'n microprocessor & microcomputer

4) What is Interrupt ?

DIRECT
address instruction
↳ needs 2 references to memory
1) Read instruction
2) Read operand

INDIRECT
address instruction
↳ needs 3 references to memory
1) Read instruction
2) Read operation
3) Read effective address